

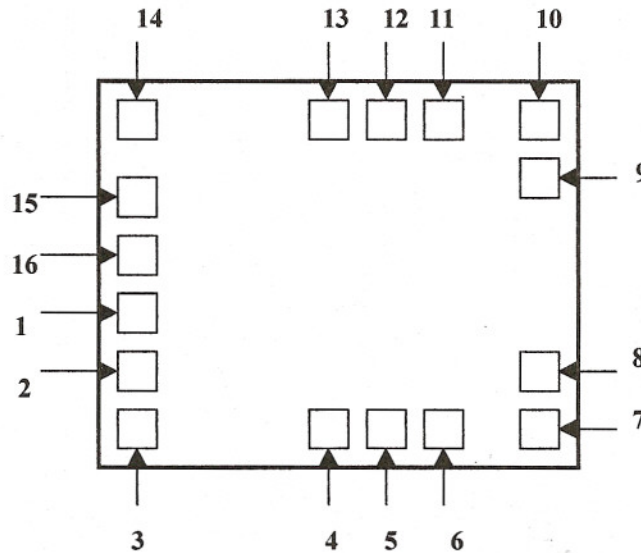


# Sierra Components, Inc.

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Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



**Topside Metal: AL**

**Backside: S1**

**Backside Potential:**

**Mask Ref: B4P**

**Bond Pads (Mils):**

**APPROVED BY:**

**MFG: Motorola**

**DIE SIZE (Mils): 75 X 28**

**THICKNESS:**

**DATE: 7/20/01**

**P/N: CD4528**